AMENDMENTS TO CLAIMS:

The listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently amended) A method comprising:

receiving a plurality of requests, each of the plurality of requests specifying an ~~one~~ address ~~in a range of multiple addresses~~;

determining if an address corresponding with one of the plurality of requests is within a ~~the~~ range of multiple addresses; and

causing a memory to be accessed whenever an address corresponding with a request is within the range of multiple addresses, the memory being identified by and accessible only through a single address, whereby the memory is accessed using any one of the addresses in the range of multiple addresses.

2. (Previously presented) The method of claim 1, further comprising sending the plurality of requests in a sequence, wherein the address corresponding with each successive request in the sequence is a successive address in the range of multiple addresses.

3. (Previously presented) The method of claim 17, wherein the memory access includes reading from the memory.

4. (Previously presented) The method of claim 17, wherein the memory access includes writing to the memory.

5. (Currently amended) An apparatus comprising:

a memory identified by and accessible only through a single address; and

at least one unit to receive a plurality of requests, each of the plurality of requests specifying an ~~one~~ address ~~in a range of multiple addresses~~, to determine if an address corresponding with one of the plurality of requests is within a ~~the~~ range of multiple addresses, and to cause the memory to be accessed whenever an address corresponding with a request is within the range of multiple addresses, whereby the memory is accessed using any one of the addresses in the range of multiple addresses.

6. (Previously presented) The apparatus of claim 5, wherein the plurality of requests are sequential and the address corresponding with each successive request in the sequence is a successive address in the range of multiple addresses.

7. (Previously presented) The apparatus of claim 5, wherein the memory access is a read access.

8. (Previously presented) The apparatus of claim 5, wherein the memory access is a write access.

9. (Currently amended) A medium readable by a machine embodying a program of instructions executable by the machine to perform a method, the method comprising the steps of:

receiving a plurality of requests, each of the plurality of requests specifying an ~~one~~ address ~~in a range of multiple addresses~~;

determining if an address corresponding with one of the plurality of requests is within a ~~the~~ range of multiple addresses; and

causing a memory to be accessed whenever an address corresponding with a request is within the range of multiple addresses, the memory being identified by and accessible only through a single address, whereby the memory is accessed using any one of the addresses in the range of multiple addresses.

10. (Previously presented) The medium of claim 9, wherein the method further comprises sending the plurality of requests in a sequence, wherein the address corresponding with each successive request in the sequence is a successive address in the range of multiple addresses.

11. (Previously presented) The medium of claim 9, wherein the memory access includes reading from the memory.

12. (Previously presented) The medium of claim 9, wherein the memory access includes writing to the memory.

13. (Currently amended) A system for burst mode data transfers, comprising:

a bus;

a processor, coupled with the bus to place a plurality of requests on the bus, each of the plurality of requests specifying an ~~one~~ address ~~in a range of multiple addresses~~;

a memory, coupled with the bus, the memory being identified by and accessible only through a single address; and

at least one unit, coupled with the bus and with the memory, to receive the plurality of requests from the bus, to determine if an address corresponding with one of the plurality of requests is within a ~~the~~ range of multiple addresses, and to cause the memory to be accessed whenever an address corresponding with a request is within the range of multiple addresses, whereby the memory is accessed using any one of the addresses in the range of multiple addresses.

14. (Previously presented) The system of claim 13, wherein the memory is a first-in-first-out memory.

15. (Previously presented) The system of claim 14, wherein the memory access is a read access.

16. (Previously presented) The system of claim 14, wherein the memory access is a write access.

17. (Previously presented) The method of claim 1 , wherein the memory is a first-in-first-out memory.

18. (Previously presented) The apparatus of claim 5, wherein the memory is a first-in-first-out memory.

19. (Currently amended) The apparatus of claim 5, wherein the apparatus is coupled with a bus, and the range of multiple addresses is predetermined and a subset of the set of addresses that may be placed on the bus.

20. (Previously presented) The medium of claim 9, wherein the memory is a first-in-first-out memory.